A study of the effects of ALD growth temperature on Al_2O_3 gate oxide by C-V and G-V measurements

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Atomic layer deposition (ALD) was used to grow aluminum oxide (Al_2O_3) on n-type Si (100) substrates at several temperatures 100-200°C. The effect of growth temperature on the Al_2O_3-Si interface was probed using capacitance-voltage (C-V) and conductance-voltage (G-V) measurements. From these measurements, oxide charge density, interface-trapped charge density, and average interface electron trap cross section were studied. As a result of incomplete experimental methods, the dependence of these parameters on growth temperature has been analyzed with only rough approximations. While the data presented here are generally inconclusive, some use might be made of the considerable number of literature results that have been summarized. Lastly, the reader should note that the present study was conducted as part of a 10-week Research Experience for Undergraduates (REU) program at UCLA.

I. INTRODUCTION

Conventional SiO_2 dielectrics in MOS structures are becoming inadequate as a result of device-miniaturization. In particular, SiO_2 layers less than ∼1nm thick admit unacceptable leakage currents [1] and limit device efficiency. Meanwhile, the prevention of leakage currents with thicker SiO_2 layers yields insufficient gate capacitance. This dilemma is the motivation behind an ongoing search for so-called high-κ alternatives to SiO_2. Due to their high permittivity, these gate dielectrics can be made thick enough to block leakage currents yet provide satisfactory gate capacitance.

Although many high-κ materials have been proposed as replacements for SiO_2, their implementation has been delayed by poor interfacial characteristics with silicon. In fact, the quality of the SiO_2-Si interface has not been surpassed by any high-κ alternative [11]. Found below is a brief annotated list of dielectric material properties necessary for high performance MOS structures. (An extensive review is given by Wilk et al. [7]).

- Thermodynamic stability: Typical high-κ dielectrics react with silicon to produce an unpredictable and often non-stoichiometric interfacial layer [7]. An intermediate passivation layer of SiO_2 is usually needed to stop reactions, but this is undesirable as it reduces gate capacitance [7].

- Appropriate coordination chemistry: Lucovsky et al. have shown that dielctrics with average coordination number of about 3 or less give the lowest density of interfacial defects [7, 12]. Ideally, defects such as fixed oxide charges and interface-traps should have densities in low ranges of 10^{10}cm^{-2} and $10^{10}\text{cm}^{-2}\text{eV}^{-1}$ respectively [6, p.2]. But in practice, high-κ materials are often too highly coordinated to bond effectively with silicon, which magnifies ideal defect densities by one or two orders of magnitude [7].

- Amorphous chemical structure: Commonly, high-κ materials have crystalline structures whose grain boundaries cause spatial dispersion in κ and provide extra avenues for leakage currents [7]. Only a few high-κ materials evade this problem via an amorphous chemical structure which interfaces smoothly with silicon and minimizes leakage currents [7].

With respect to all three of the material properties listed above, Al_2O_3 is one of the most promising high-κ dielectrics. Despite the fact that Al_2O_3 has been studied for a long time, progress in low temperature ALD methods has aroused interest in the relationships between deposition conditions and the electrical properties of Al_2O_3 [10, 13–15]. Such interest can be attributed to the fact that performing ALD at sufficiently low temperatures (<300°C) prevents degradation of semiconductor device components [2]. A summary of the variation of Al_2O_3 properties with ALD growth temperature, as determined from previous studies, may be found in Table I. All table entries reflect ALD growths using Trimethylaluminum (TMA) and water precursors on silicon substrates, but some differences in growth conditions exist between the references (particularly the number of ALD cycles). Also keep in mind that the table entries have been roughly estimated in some cases and are only intended to depict general trends.

In addition to the those listed in Table I, other Al_2O_3 properties have been studied for their dependence on ALD growth temperature. Indeed, enough work on this topic has been done in order to suggest that the electrical properties of Al_2O_3 are optimized by growths at 350°C [13]. Furthermore, a study conducted by Drozd et al. has already provided results on some of the growth-temperature-dependent parameters to be considered here [8]. Their report on ∼100nm Al_2O_3 layers demonstrated that oxide trapped charge density decreases monotoni-

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TABLE I: The Dependence of Al_2O_3 Properties on ALD Growth Temperature

Al_2O_3 Property	Temperature (°C)					
	33	150	177	250	400	500
Growth Rate (Å/cycle)	1.1 [10]	∼0.75 [15]	1.25 [10]	1 [14]	0.8 [14]	0.6 [15]
%H-atom Impurity	21.7 [10]		6.9 [10]	8.5 [14]	3.0 [14]	
Refractive Index	1.51 [10]	1.63 [15]	1.60 [10]	1.64 [14]	1.67 [14]	1.67 [15]
Dielectric Constant	∼7.7 [10]	∼6.3 [13]	∼7.7 [10] 6.7 [13]	8.2 [15]	∼6.8 [13]	
Density (g/cm^3)	2.5 [10]		3.0 [10]			

cally from $\sim 17\times10^{11}cm^{-2}$ to $\sim 7\times10^{11}cm^{-2}$ as growth temperature increases 150-310°C (for large positive measurement biases). Similary, they found that the density of oxide electron traps decreases monotonically between $2\times10^{12}cm^{-2}$ and $1\times10^{12}cm^{-2}$ with increasing growth temperature (hole trap density reportedly shows opposite behavior). Lastly, they reported qualitatively that catastrophic breakdown voltage decreases with decreasing growth temperature.

It is the purpose of the present study to build on the results of Drozd et al. This will be done by employing G-V measurements to study interface-trap cross section dependence on ALD growth temperature, which was not done in that report. Also, the ∼11nm oxide layers studied here were fabricated using current ALD technology, which is significant given that Drozd paper was published in 1994.

II. EXPERIMENTAL

Fabrication

In order to study the effect of ALD growth temperature on the Al_2O_3-Si interface, five MOS capacitors were fabricated using Al_2O_3 layers grown at 100°C, 135°C, ∼170°C, and 200°C (two growths at 200 °C). The growth at ∼170°C actually ranged between 160°C and 180°C, but all other growths occurred at fixed temperature. Each sample was prepared with a separate phosphorous-doped Si (100) substrate having resistivity less than 0.01 ohm-cm. In every case, 100 ALD cycles were carried out on a Savannah 100-Cambridge Nanotech Inc. instrument using alternating pulses (0.05 sec.) of TMA and water, with nitrogen purges (5 sec.) between the pulses. According to the instrument manual, each cycle generates a layer no thicker than 1.1Å. Thus, it is assumed that the 100-cycle process produced layers no thicker than ∼11nm. The deposition conditions were automatically controlled using instrument supplied software. After completion of the ALD process, an SPI-Module^{TM} Sputter Coater was used to deposit $\sim 1mm^2$ gold electrodes on the Al_2O_3 layers. The sputtering was performed with a DC argon plasma set at 18mA for 360 sec. Finally, two electrical contacts were made to each sample: 32 gauge copper wires were silver-epoxied to each gold electrode and to the back of each substrate. The epoxy was prepared using Epoxy Technology H20E Parts A-B and the epoxied wires were baked for ∼45 min. at 100°C.

Measurement

A two-terminal measurement setup was made by soldering the two contact wires of each MOS capacitor to female BNC connectors. The device under test (DUT) was shielded in a metal box and connected to an Andeen-Hagerling 2500A bridge for capacitance and conductance measurements. Also, the bridge was connected to a Stanford Research Systems SR830 DSP lock-in amplifier for external voltage supply. An automated voltage ramp (-6 to +6V) was then used to bias the DUT with a step size of 100mV (Voltages in excess of ±6V routinely caused catastrophic breakdown.). After each step, a 2.25 sec. delay was set for capacitance and conductance to be measured from the bridge (measurement circuit shown in Fig. 1). Such measurements were made at room temperature with an excitation voltage less than 250mV and a frequency of 1kHz.

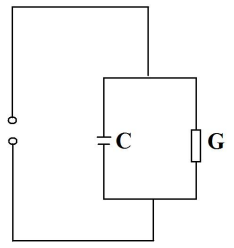

FIG. 1: Configuration of measured capacitance C and conductance G.

III. RESULTS AND DISCUSSION

C-V Measurements

The C-V plots generated by the five MOS capacitors are useful for assessing the relationship between ALD growth

temperature and densities (cm^{-2}) of oxide charges Q_{ox} and interface-trap charges Q_{it}. Several types of charge comprise Q_{ox}, including fixed oxide charge, oxide trapped charge, and mobile ionic charge (e.g. Na^{+}). Altogether, these different charges are significant to the performance of MOS devices, especially for their impact on threshold voltage. Commonly, comparisons of Q_{ox} between samples are made by extracting the flatband voltage V_{FB} from their respective C-V plots. This is possible because V_{FB} depends linearly on Q_{ox}, as well as Q_{it} [6, p.466][17]:

$$V_{FB} = -\frac{Q_{ox} + Q_{it}}{C_{ox}} + W_{ms} \tag{1}$$

where C_{ox} is the oxide capacitance (pFcm^{-2}) and W_{ms} is the work function difference between the gate metal and the substrate. Often, the influence of Q_{it} can be isolated by an annealing procedure that makes Q_{it} negligible compared to Q_{ox} [6, p.786]. In this way, V_{FB} becomes a measure of Q_{ox}. Unfortunately, the necessary annealing process was not available for this study, and as a result, the extracted V_{FB} values will only provide a comparison of $(Q_{it} + Q_{ox})$ between the samples. The usefulness of this information is limited by the fact that Q_{it} and Q_{ox} usually have opposite polarity, and thus, a single V_{FB} value will correspond to many possible charge configurations in a sample. Since only a relative comparison of $(Q_{ox} + Q_{it})$ between each sample is desired, W_{ms} is irrelevant (same gate metal and substrate material were used for all samples). Also, to a first approximation, C_{ox} may be considered the same for each sample given that the normalized capacitance plots agree closely in accumulation (c.f. Fig. 2).

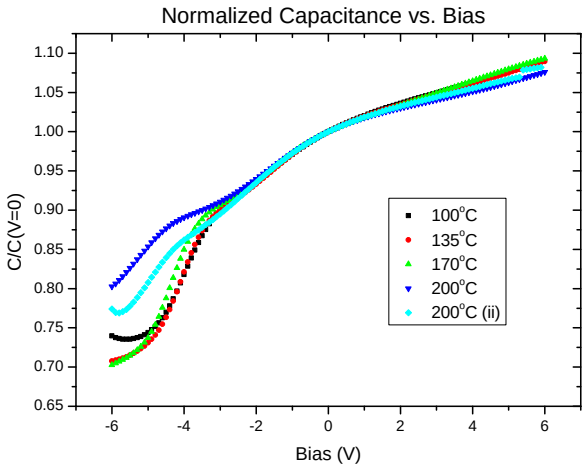

FIG. 2: To compensate for the differences in gate area between samples, the measured capacitances have been normalized by the capacitance at zero gate voltage.

The value of V_{FB} for each capacitor is now obtained by transforming its C-V plot into a Mott-Schottky plot

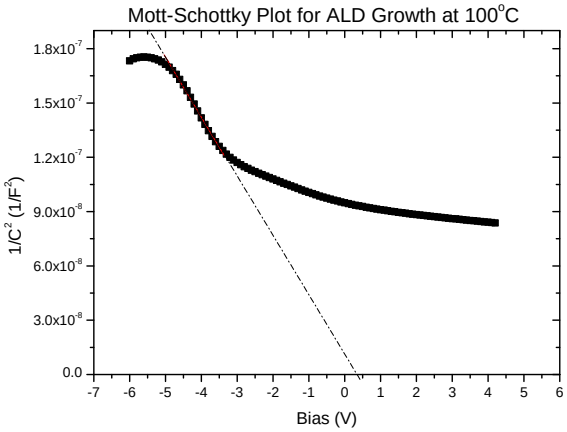

FIG. 3: The x-intercept of the extrapolated line is nearly equal to the "built-in potental" ($-V_{FB}$), while the extrapolated slope is proportional to the substrate dopant density N_d. Note that the unit of the y-axis is incorrect as shown, and should be pF^{-2}.

(e.g. Fig. 3). For large reverse bias, the Mott-Schottky plot is approximated by a line whose x-intercept yields V_{FB} from the following relation (for an n-type substrate) [3]:

$$C^{-2} = \frac{2(V_g - \psi_0 - \frac{kT}{q})}{N_d q \epsilon_s}. \tag{2}$$

So, at the x-intercept,

$$V_{FB} = -\psi_0 = \frac{kT}{q} - V_{intercept}. \tag{3}$$

Here, V_g is the gate bias, ψ_0 is the silicon surface potential at $V_g = 0$, ϵ_s is the permitivity of silicon ($\sim$1pFcm^{-1}), and at room temperature kT/q is taken to be about 0.025V. The error in V_{FB} associated with fitting a line to the linear region of the Mott-Schottky plot is estimated to be roughly 0.25V. Compounded with this fitting error, it must be noted that the Mott-Schottky plot is based on an inexact theory [5] and that the resulting V_{FB} value should be regarded as an estimate. Happily, because the slope of the extrapolated line $(d(C^{-2})/dV)$ can be used to calculate the known substrate dopant density N_d , it is possible to evaluate the reasonableness of the extrapolation [3]:

$$N_d = \frac{2}{q\epsilon_s |d(C^{-2})/dV|}. \tag{4}$$

The phosphorous dopant density was determined from the substrate resistivity to be at least $4.7\times10^{18}\mathrm{cm}^{-3}$ using a plot from the literature [9]. In comparison, the average slope of the five Mott-Schottky plots shows N_d to be about $3\times10^{18}\mathrm{cm}^{-3}$, implying that the extrapolation is sensible. However, it seems that the C-V plots do

TABLE II: ALD Growth Temperature Impact on V_{FB}

Temperature (°C)	V_{FB} (V)
100	-0.30
135	-0.37
170	0.93
200	-3.63
200 (trial ii)	-1.64

not support this conclusion, for they show that strong inversion is not reached until ∼-5V, and likewise, that V_{FB} values should be much lower than those obtained from the extraction (Table II). For reference, a V_{FB} of 0.3V might be expected from an n-type sample reaching strong inversion at ∼-1V [13].

As shown in Table II, there is no obvious relationship between ALD growth temperature and V_{FB}. It should be pointed out that the differences in V_{FB} values from the table would cause pronounced shifts between the curves of the normalized capacitance plot (which are not present). For this reason, the data in Table II should be treated with skepticism. In other words, the absence of shifts between the curves of Fig. 3 implies that (Q_{ox}+Q_{it}) does not vary appreciably between the samples [6, p.427].

Analogous results have been reported by Groner et al. [13], who compared V_{FB} values obtained by C-V and I-V measurements on Al_2O_3 layers grown under a variety of ALD conditions. Specifically, they found that V_{FB} values obtained from C-V measurements varied between 0-1.5V, while I-V measurements produced fairly constant V_{FB} values [13]. Notably, the C-V plot given in that report for a 120Å thick Al_2O_3 layer grown at 177°C is much more ideal in appearance than the plot presented here for a similar sample. Since Groner et al. mentioned that sample preparation with a class-100 cleanroom had a significant effect on the insulating properties of Al_2O_3, the non-ideal C-V plots here may be due to the use of less clean methods.

G-V Measurements

The most prominent feature of the G-V plot for MOS devices is a peak, located near the depletion regime. Because depletion conductance (for n-type substrates) is dominated by the effects of interface electron traps [6, p.100], the G-V peak offers insight into their properties, particularly their average capture cross-section σ_n (with unit cm^{-2} and averaging over the energetic distribution of traps). The following explanation for the origin of the G-V peak has been provided by Nicollian, Goetzberger, and Brews [4][6, p.291]. To begin, the average surface potential ψ (volts) controls the interface carrier density N_i. The greater (lower) N_i is, the more quickly (slowly) interface-traps may be filled (when this is energetically favorable). Next, when an AC test signal is superimposed on the DC bias, the energy levels of the interface-traps fluctuate with respect to the Fermi level, at a rate dictated by the measurement frequency. For very large (very small) N_i, charge capture rates are fast (slow) compared to the AC frequency and the resulting loss is minor. But when N_i is tuned so that the characteristic time τ of charge capture matches the period the AC signal, a peak in conductance is observed.

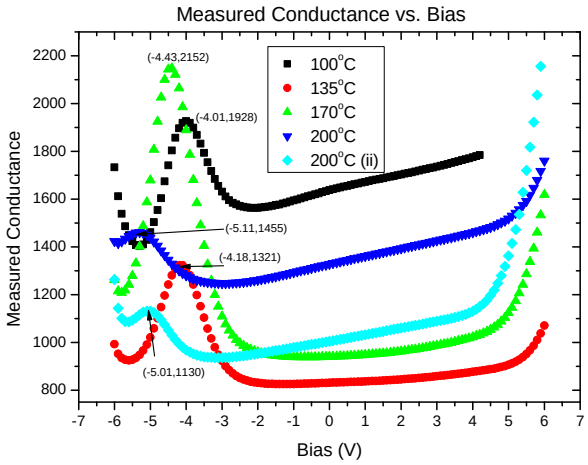

FIG. 4: V_{peak} decreases monatonically with increasing ALD growth temperature. This enables σ_n to be studied as function of the growth temperature. Note that the unit of the y-axis should be nanosiemens (nS).

Since a 1kHz signal was used for all measurements, the surface potential corresponding to peak conductance ψ_{peak} will give about the same value of τ for all samples. This fact is useful because it allows τ for each sample to be equated (when τ is evaluated at ψ_{peak}). Moreover, using the equation below, $\sigma_n@\psi_{peak}$ may be calculated with $\tau@\psi_{peak}$, thus allowing for comparison of the depletion value of σ_n between samples [6, p.212]:

$$\sigma_n = \frac{e^{-\psi/\beta}}{\tau v_{th} N_d}, \tag{5}$$

where v_{th} is the thermal carrier velocity, and $\beta := kT/q$. To quantitatively extract σ_n from this relation, ψ would have to be known accurately as a function of gate bias. Even though such information is not available, it may be assumed that ψ is related to the gate bias by [18][6, p.94],

$$\psi = V_g(1 + \frac{C_w}{C_{ox}}) - V_{FB} + K, \tag{6}$$

where C_w is a parasitic measurement capacitance, and K depends on C_{ox} as well as two device independent parameters [6, p.94]. From the G-V plot, the gate bias V_{peak}, corresponding to maximum G, increases as growth temperature decreases. Applying this to (6) and (5), we see qualitatively that as growth temperature decreases,

V_{peak} becomes less negative, and $\sigma_n@V_{peak}$ decreases (assuming for the moment that ψ is controlled primarily by V_g while V_{FB} and K are negligible). Now, to make the relationship between σ_n and growth temperature more precise, we take the ratio R of the cross section values $\sigma_{n,100C}$ and $\sigma_{n,200C}$ corresponding to highest and lowest growth temperatures:

$$R := \frac{\sigma_{n,100C}}{\sigma_{n,200C}} = \frac{e^{-(M\Delta V - V_{FB,100C})/\beta}}{e^{V_{FB,200C}/\beta}}. \qquad (7)$$

The following quantities have been defined here for simplicity: $M := 1 + \frac{C_w}{C_{ox}}$, $\Delta V := V_{peak,100C} - V_{peak,200C}$. In addition, (7) has been obtained by assuming that N_i, v_{th}, and C_{ox} are about the same for each sample (in depletion). The first two assumptions are reasonable since all measurements were made at the same temperature, and on the same type of substrate. The latter is justified if we suppose that C_{ox} does not change much with bias, since C_{ox} was already explained to be about the same for all samples in accumulation. Lastly, because of the absence of relative shifts in the normalized C-V plots, we will also assume that V_{FB} is the same for all samples. Now, observing from the G-V plots that $\Delta V \approx 1$V, and that at room temperature $\beta \approx 0.025$V, we may plug all of the known parameters into (7) to get,

$$R \approx e^{-40M}. \qquad (8)$$

Because M is probably not much greater than 1, (8) shows that $\sigma_{n,100}$ is catastrophically less than $\sigma_{n,200}$ by about 18 orders of magnitude! This is clearly unreasonable. For comparison, interface-trap capture cross section measurements (at a single trap energy level) on the Si-SiO_2 system have been shown to vary by as much as four orders of magnitude, depending possibly on preparation methods [16]. However, such dispersion in σ_n does not always occur, even for significantly different SiO_2 oxidation conditions [16]. Consequently, it may not even be true that σ_n decreases (in depletion) with decreasing growth temperature (which would seem quite obvious when (5) is evaluated at V_{peak} for different samples). At the very least, this analysis indicates that plausible changes in σ_n are not sufficient to account entirely for the observed G-V peak shifting. Hence, additional factors should be considered in future studies.

IV. CONCLUSION

The influence of ALD growth temperature on oxide charge density (Q_{ox}), interface-trapped charge density (Q_{it}), and average electron capture cross section (σ_n) has been analyzed for the Al_2O_3-Si system. Based on the absence of shifting in normalized C-V plots for ∼11nm Al_2O_3 layers grown at several temperatures (100-200°C), it appears that $Q_{ox}+Q_{it}$ does not vary much with growth temperature. Meanwhile, G-V plots were shifted monatonically to the right (∼1V in total) as growth temperature decreased. Although such shifting may have been caused in part by decreasing σ_n with decreasing growth temperature, the analysis has shown that σ_n cannot reasonably account for it entirely.

Acknowledgement

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[17] The equation from Nicollian and Brews has been modified slightly by incorporating mobile oxide charges and oxide trapped charges with Q_f, as on p.466.

[18] The band bending expressed by Nicollian and Brews on p.94 is taken to be an average value here so that (6) may be substituted into (5).